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UNITED STATES PATENT APPLICATION

For

AN ELECTRONIC ASSEMBLY HAVING A WETTING LAYER ON A THERMALLY CONDUCTIVE HEAT SPREADER

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AN ELECTRONIC ASSEMBLY HAVING A WETTING LAYER ON A THERMALLY CONDUCTIVE HEAT SPREADER

BACKGROUND OF THE INVENTION

1). Field of the Invention

[0001] This invention relates to an electronic assembly of the kind having a semiconductor die which is thermally coupled through an interface material to a thermally conductive heat spreader.

2). Discussion of Related Art

[0002] Integrated circuits are manufactured on semiconductor wafers which are subsequently sawed or "diced" into individual dice. Such a die may have solder bump contacts on the integrated circuit. The solder bump contacts are located downward onto contact pads of a package substrate, and attached in a thermal reflow process. Electronic signals can be provided through the solder bump contacts to and from the integrated circuit. Operation of the integrated circuit causes heating thereof. Heat is conducted to an upper surface of the die, and has to be conducted or convected away to maintain the temperature of the integrated circuit below a predetermined level for purposes of maintaining functional integrity of the integrated circuit.

[0003] A heat spreader is usually located above the die and thermally coupled

to the die by means of a thermal interface material such as thermally conductive grease. The thermally conductive grease transfers minimal stresses from the heat spreader to the die, but has a relatively low thermal conductivity and thus provides a substantial barrier for heat transferring from the die to a heat spreader.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The invention is described by way of example, with reference to the accompanying drawings, wherein:

[0005] Figure 1 is a cross-sectional side view of components of an electronic assembly, before being finally assembled;

[0006] Figure 2 is a view similar to Figure 1, after final assembly of the components of the electronic assembly; and

[0007] Figure 3 is a cross-sectional side view illustrating components of the electronic assembly of Figure 2 in greater detail.

DETAILED DESCRIPTION OF THE INVENTION

[0008] Figure 1 of the accompanying drawings illustrates components of an electronic assembly 10, before being finally assembled, including a semiconductor package subassembly 12, a preform of pure indium 14, a heat spreader subassembly 16, and an adhesive 18.

[0009] The heat spreader subassembly 16 includes a primary heat spreading structure 20 of copper, a thin nickel layer 22 plated on the primary heat spreading structure 20, and a gold layer 24 plated on the nickel layer 22.

[0010] The primary heat spreading structure 20 includes a horizontal heat spreading plate 28, and sides 30 extending downward from edges of the heat spreading plate 28. There are four of the sides 30 which, together with the heat spreading plate 28, form an inverted cap with an internal cavity 32 which is open to the bottom. All surfaces of the primary heat spreading structure 20 are plated with the nickel layer 22. The nickel layer 22 is thus also plated on a lower surface of the heat spreading plate 28.

[0011] The gold layer 24 is selectively plated on an area of the nickel layer 22, located on the lower surface of the heat spreading plate 28. The gold layer 24 may be formed by first masking surfaces of the nickel layer 22 where the gold layer 24 is not required, plating on exposed surfaces of the nickel layer 22, and subsequently removing any masking material on surfaces of the nickel layer 22

where the gold layer 24 is prevented from plating. The gold layer 24 has an optimal thickness, which will be discussed hereinbelo w.

[0012] The semiconductor package subassembly 12 includes a package substrate 36 and a semiconductor die 38. The package substrate 36 is typically primarily made of an organic plastics material. The semiconductor die 38 includes a semiconductor substrate 40 having an integrated circuit 42 of semiconductor electronic components and metal lines in a lower surface thereof.

[0013] The semiconductor die 38 further includes solder bumps 44 formed on a lower surface of the integrated circuit 42. The solder bumps 44 are typically formed according to the known controlled collapse chip connect (C4) process. The solder bumps 44 are structurally secured to the semiconductor substrate 40 in a known reflow process. The solder bumps 44 are also electrically connected to the integrated circuit 42, so that signals can be provided through the solder bumps 44 to and from the integrated circuit 42. The semiconductor die 38 also includes a stack 46 of layers formed on an upper surface of the semiconductor substrate 40. The stack 46 includes titanium, a nickel vanadium alloy, and gold layers, which are sequentially deposited on top of one another. The preform of indium 14 is approximately 1 mm thick, has a thermal conductivity of approximately 80 W/mK, and is located on an upper surface of the gold layer of the stack 46.

[0014] The adhesive 18 is located on lower surfaces of the sides 30. The heat

spreader subassembly 16 is located over the semiconductor die 38 and the preform of indium 14. Lower surfaces of the adhesive 18 contact an upper surface of the package substrate 36. A lower surface of the gold layer 24 contacts an upper surface of the preform of indium 14.

[0015] A clamp (not shown) is then located over the components of the electronic assembly 10, and the electronic assembly 10, together with the clamp, is sent through a reflow furnace. The components of the electronic assembly 10 are heated in the reflow furnace, and subsequently allowed to cool. The reflow furnace heats the components of the electronic assembly 10 to a temperature of, for example, approximately 170°C. Such a temperature is above a melting temperature of pure indium of approximately 157°C, so that the indium 14 melts.

[0016] Figure 2 illustrates the electronic assembly 10 after it is allowed to cool. Cooling of the indium 14 causes its solidification. By heating and cooling the indium 14, the indium is "soldered" to both the gold layer 24 and the gold layer of the stack 46. The indium 14 thereby forms a layer which secures the stack 46 structurally to the gold layer 24, and which provides a highly effective path for heat to conduct from the stack 46 to the gold layer 24. The sides 30 are also secured to the substrate 36 by the adhesive 18. It should be noted that wetting does not occur because the gold layer is heated to above its melting temperature. Gold has a melting temperature of 1065°C. The gold layer 24 thus promotes wetting although the assembly is heated to 170°C and the temperature is

reversed without going over 170°C.

[0017] The purpose of the gold layer 24 is to serve as a wetting layer for the indium 14. Gold is a better wetting layer than nickel, hence the reason why the indium 14 is not located directly against the nickel 22. A better structural and thermal connection is formed by the use of the gold layer 24. The nickel layer 22, for purposes of the present invention, serves to act as a diffusion barrier preventing cross-diffusion between the gold layer 24 and the copper of the primary heat spreading structure 20.

[0018] Figure 3 is a cross-sectional view showing the components of the assembly 10 of Figure 2 in greater detail. Some of the gold layer 24 and some of the indium 14 are consumed to form an $AuIn_2$ intermetallic layer 50 between the remaining gold layer 24 and the remaining indium 14. An $AuIn_2$ intermetallic is preferred, although other Au-In intermetallics may, and probably do, get formed. A similar $AuIn_2$ intermetallic layer 52 is formed by the gold layer of the stack 46 and the indium 14. The electronic assembly 10 is subsequently alternatingly heated and cooled in a reliability test. It has been found that when the gold layer 24 is approximately three microns thick before being located in the reflow oven, the reliability test allows for 50 cycles of thermal cycling before significant thermal degradation is detected in the tri-layer 46, 14 and 24. If the gold layer 24 is not present, delamination occurs in the first cycle. It was also found that when the gold layer 24 is approximately 0.2 microns thick, cracking

only occurs after 200 cycles, often only after 300 cycles. When a thinner gold layer is plated, a thinner intermetallic layer 50 is created than when a thicker gold layer is plated. A thinner intermetallic layer can withstand a larger number of thermal cycles in a given reliability test than a thicker intermetallic layer. Ideally, the gold layer 24 should have substantially no porosity. It has been found that a uniform gold layer as this as 0.02 microns can be formed with substantially no porosity.

[0019] The reliability test that was used was as follows:

[0020] The temperature was ramped up to 125°C and held at such temperature for 15 minutes. The temperature was then lowered to -55°C and held at such temperature for 15 minutes to complete one cycle. The temperature was then again increased to 125°C, the beginning of a second cycle. The remainder of the second cycle was identical to the first cycle, and subsequent cycles were identical to the first cycle.

[0021] Referring again to Figure 2, portions of the gold layer 24 to the left and right of the indium 14 remain unreacted with the indium 14, and thus maintain their thickness as shown in Figure 1.

[0022] Other materials may be used instead of the gold layer 24 to provide a wetting layer over the nickel layer 22. Such materials include tin and noble metals such as silver and palladium, or combinations of these metals. Tin, silver, and palladium have melting temperatures of 2260°C, 961°C, and 1552°C

respectively. It was found that silver with a thickness of approximately 0.2 or less microns is optimal. It may also be possible to make the primary heat spreading structure 20 of other materials such as aluminum, and have nickel plated on the aluminum. Materials other than the pure indium 14 may also be possible, but such a material preferably has a thermal conductivity of at least 35 W/mK, although a thermal conductivity of at least 70 W/mK is much preferred.

[0023] In use, electronic signals are transmitted through the solder bumps 44 between the package substrate 36 and the integrated circuit 42. Operation of the integrated circuit 42 causes heating of the semiconductor die 38. Heat transfers from the semiconductor die 38 through the indium 14 to the heat spreader subassembly 16. The heat spreads sideways through the heat spreader subassembly 16 and is conducted or convected from an upper surface of the heat spreader subassembly 16.

[0024] While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not restricted to the specific constructions and arrangements shown and described since modifications may occur to those ordinarily skilled in the art.